Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (cancelled)

2. (cancelled)

3. (cancelled)

4. (currently amended) A method for customizing a network processor; comprising the steps of:

(a) providing at least one field programmable gate array (FPGA) cell and a plurality of standard cells within the network processor;

(b) providing a custom logic file for [the] a vendor of the network processor by a customer of the network processor wherein step (b) further comprises (b1) providing a verification module within the custom logic file; and

(c) programming the at least one FPGA cell[,] by the vendor based upon the custom logic [bill] cell to provide a customized network processor; and

d verifying the customized network processor based upon the verification module.

5. (cancelled)

6. (cancelled)

7. (currently amended) A network processor comprising:

a plurality of standard cells, the plurality of standard cells comprising common logic;

a plurality of FPGA cells, the plurality of FPGA cells comprising high risk logic; and

~~at least one bus coupled to a portion of the standard cells and portion of the FPGA cells, wherein each of the plurality of FPGA cells allows for customization of the network processor~~ a processor first bus and two peripheral buses coupled to a portion of the standard cells and portion of the FPGA cells, wherein the FPGA cells coupled to the first bus comprise an accelerator function and a second function; wherein the FPGA cells coupled to one of the two peripheral buses are interfaces; wherein the FPGA cells coupled to the other of the two peripheral buses are a third function and a fourth function; wherein the plurality of cells each can provide a specified function based upon field programming techniques to allow for customization of the network processor.

8. (cancelled)

9. (cancelled)

10. (currently amended) The network processor of claim 7 wherein the FPGA cells coupled to the ~~PLB~~ first bus comprise an accelerator function and a ~~PLB~~ first master/slave function.

11. (currently amended) The network processor of claim 7 wherein the FPGA cells coupled to one of the two ~~OPBs~~ peripheral busses are media interfaces.

12. (currently amended) The network processor of claim 7 wherein the FPGA cells coupled to the other of the two ~~OPBs~~ peripheral busses are a GPIO preprocessor function and ~~an OPB~~ a peripheral bus master/slave function.

13. (original) A network processor comprising:

a plurality of standard cells, the plurality of standard cells comprising common logic;

a plurality of FPGA cells, the plurality of FPGA cells comprising high risk logic; and

a processor local bus (PLB) and two on-chip peripheral buses (OPBs) coupled to a portion of the standard cells and portion of the FPGA cells, wherein the FPGA cells coupled to the PLB comprise an accelerator function and a PLB master/slave function; wherein the FPGA cells coupled to one of the two OPBs are media interfaces; wherein the FPGA cells coupled to the other of the two OPBs are a GPIO preprocessor function and an OPB master/slave function; wherein the plurality of cells each can provide a specified function based upon field programming techniques to allow for customization of the network processor.